CLAIMS

1. Bridge apparatus for connecting a first multimaster bus I^2C environment to a second multimaster bus I^2C environment, comprising

an address bitmap having a value associated with each possible I^2C address;

a port-A interface that receives address signals and data signals from the first multimaster and transmits data signals to the first multimaster bus;

a port-B interface that transmits address signals and data signals to the second multimaster bus and received data signals from the second multimaster bus; and

a controller that selectively passes an address and data received on the port-A interface from the first multimaster bus to the port-B interface for transmission on the second multimaster bus depending on the address bitmap value associated with the address.

2. The bridge apparatus of claim 1 wherein the controller comprises a command interpreter that receives commands at the port-A interface from the first multimaster bus and controls the operation of the bridge apparatus in response to received commands.

3. The bridge apparatus of claim 2 wherein a tunnel command received by the bridge apparatus includes a tunnel address and the controller passes the tunnel address to the port-B interface for transmission on the second multimaster bus.

4. The bridge apparatus of claim 2 further comprising a plurality of registers, each holding a value that control the operation of the bridge apparatus and wherein the command interpreter receives commands at the port-A interface from the first

multimaster bus and places a value in at least one of the registers in response thereto.

5. The bridge apparatus of claim 4 wherein a first register holds a bridge ID value and each command contains a bridge ID value and wherein the command interpreter comprises a mechanism which responds to a command when the bridge ID value therein equals the bridge ID in the first register.

6. The bridge apparatus of claim 5 wherein a second register defines a range of bridge IDs and wherein the command interpreter comprises another mechanism that transmits a received command on the second multimaster bus when the bridge ID in the received command is in the range of bridge IDs.

7. The bridge apparatus of claim 1 wherein the controller is a programmed microcontroller.

8. The bridge apparatus of claim 7 wherein the micocontroller comprises a RAM memory wherein the address bitmap is located.

9. The bridge apparatus of claim 7 wherein the microcontroller is connected to the port-A interface by a clock and data line and the microcontroller detects a START signal by generating an interrupt based on a signal on the data line.

10. Bi-directional bridge apparatus for connecting a first multimaster bus I^2C environment and a second multimaster bus I^2C environment, comprising

a first unidirectional bridge device having, a first address bitmap having a value associated with each possible I^2C address, a first port-A interface that receives address and data signals from the first multimaster bus, a first port-B

interface that transmits address and data signals to the second multimaster bus; and a first controller that selectively passes an address and data received on the port-A interface from the first multimaster bus to the port-B interface for transmission on the second multimaster bus depending on the first address bitmap value associated with the address and

a second unidirectional bridge device having, a second address bitmap having a value associated with each possible I^2C address, a second port-A interface that receives address and data signals from the second multimaster bus, a second port-B interface that transmits address and data signals to the first multimaster bus; and a second controller that selectively passes an address and data received on the port-A interface from the second multimaster bus to the port-B interface for transmission on the first multimaster bus depending on the second address bitmap value associated with the address.

11. The bi-directional bridge apparatus of claim 10 wherein both the first and second unidirectional bridge devices have a mechanism for designating whether a unidirectional bridge device is one of an upstream bridge and a downstream bridge.

12. The bi-directional bridge apparatus of claim 10 further comprising a deadlock mechanism for choosing one of the unidirectional bridge devices when both unidirectional bridge devices simultaneously begin a transaction.

13. The bi-directional bridge apparatus of claim 10 wherein the first unidirectional bridge device further comprises a plurality of registers, each holding a value that control the operation of the first unidirectional bridge device and wherein the first controller comprises a first command interpreter that receives commands at the port-A interface from the first multimaster bus and places a value in at least one of the registers in response thereto.

14. The bi-directional bridge apparatus of claim 13 wherein each of the commands contains a bridge ID and at least one of the registers defines a range of bridge IDs and wherein the first command interpreter comprises a mechanism that transmits a received command on the second multimaster bus when the bridge ID in the received command is in the range of bridge IDs.

15. The bi-directional bridge apparatus of claim 10 wherein the second unidirectional bridge device further comprises a plurality of registers, each holding a value that control the operation of the second unidirectional bridge device and wherein the second controller comprises a second command interpreter that receives commands at the port-A interface from the second multimaster bus and places a value in at least one of the registers in response thereto.

16. The bi-directional bridge apparatus of claim 15 wherein each of the commands contains a bridge ID and at least one of the registers defines a range of bridge IDs and wherein the second command interpreter comprises a mechanism that transmits a received command on the first multimaster bus when the bridge ID in the received command is outside the range of bridge IDs.

17. The bi-directional bridge apparatus of claim 15 wherein a register in the first unidirectional bridge device holds a first bridge ID value and a register in the second unidirectional bridge device holds a second bridge value different from the first bridge ID value.

18. The bi-directional bridge apparatus of claim 13 wherein each command contains a bridge ID value and wherein the first command interpreter comprises a mechanism which responds to a command when the bridge ID value therein equals the bridge ID in the first register.

19. The bi-directional bridge apparatus of claim 17 wherein each command contains a bridge ID value and wherein the second command interpreter comprises a mechanism which responds to a command when the bridge ID value therein equals the bridge ID in the first register.

20. A method for connecting a first multimaster bus I^2C environment to a second multimaster bus I^2C environment, comprising

(a) connecting the first multimaster bus to the second multimaster bus with a bridge having an address bitmap having a value associated with each possible I^2C address, a port-A interface that receives address signals and data signals from the first multimaster and transmits data signals to the first multimaster bus and a port-B interface that transmits address signals and data signals to the second multimaster bus and received data signals from the second multimaster bus; and

(b) selectively passing an address and data received on the port-A interface from the first multimaster bus to the port-B interface for transmission on the second multimaster bus depending on the address bitmap value associated with the address.

21. The method of claim 20 wherein step (b) comprises receiving commands at the port-A interface from the first multimaster bus and controlling the operation of the bridge apparatus in response to received commands.

22. The method of claim 21 wherein a tunnel command received by the bridge apparatus includes a tunnel address and wherein step (b) further comprises passing the tunnel address to the port-B interface for transmission on the second multimaster bus.

23. The method of claim 21 wherein the bridge further comprises a plurality of registers, each holding a value that control the operation of the bridge apparatus and wherein step (b) comprises receiving commands at the port-A interface from the first multimaster bus and places a value in at least one of the registers in response thereto.

24. The method of claim 23 wherein a first register holds a bridge ID value and each command contains a bridge ID value and wherein step (b) comprises responding to a command when the bridge ID value therein equals the bridge ID in the first register.

25. The method of claim 24 wherein a second register defines a range of bridge IDs and step (b) comprises transmitting a received command on the second multimaster bus when the bridge ID in the received command is in the range of bridge IDs.

26. The method of claim 20 wherein the bridge comprises a programmed microcontroller that performs step (b).

27. The method of claim 26 wherein the micocontroller comprises a RAM memory wherein the address bitmap is located.

28. The method of claim 26 wherein the microcontroller is connected to the port-A interface by a clock and data line and the microcontroller detects a START signal by generating an interrupt based on a signal on the data line.

29. A method for connecting a first multimaster bus I^2C environment and a second multimaster bus I^2C environment, comprising

(a) connecting the first multimaster bus to the second multimaster bus with a first unidirectional bridge device having a first address bitmap having a value associated with each possible I^2C address, a first port-A interface that receives address and data signals from the first multimaster bus, a first port-B interface that transmits address and data signals to the second multimaster bus;

(b) selectively passing an address and data received on the port-A interface from the first multimaster bus to the port-B interface for transmission on the second multimaster bus depending on the first address bitmap value associated with the address;

(c) connecting the second multimaster bus to the first multimaster bus with a second unidirectional bridge device having, a second address bitmap having a value associated with each possible I^2C address, a second port-A interface that receives address and data signals from the second multimaster bus, a second port-B interface that transmits address and data signals to the first multimaster bus; and

(d) selectively passing an address and data received on the port-A interface from the second multimaster bus to the port-B interface for transmission on the first multimaster bus depending on the second address bitmap value associated with the address.

30. The method of claim 29 wherein both the first and second unidirectional bridge devices have a mechanism for designating whether a unidirectional bridge device is one of an upstream bridge and a downstream bridge.

31. The method of claim 29 further comprising a deadlock mechanism for choosing one of the unidirectional bridge devices when both unidirectional bridge devices simultaneously begin a transaction.

32. The method of claim 29 wherein the first unidirectional bridge device further comprises a plurality of registers, each holding a value that control the operation of the first unidirectional bridge device and wherein step (b) comprises receiving commands at the port-A interface from the first multimaster bus and placing a value in at least one of the registers in response thereto.

33. The method of claim 32 wherein each of the commands contains a bridge ID and at least one of the registers defines a range of bridge IDs and wherein step (b) comprises transmitting a received command on the second multimaster bus when the bridge ID in the received command is in the range of bridge IDs.

34. The method of claim 29 wherein the second unidirectional bridge device further comprises a plurality of registers, each holding a value that control the operation of the second unidirectional bridge device and wherein step (d) comprises receiving commands at the port-A interface from the second multimaster bus and placing a value in at least one of the registers in response thereto.

35. The method of claim 34 wherein each of the commands contains a bridge ID and at least one of the registers defines a range of bridge IDs and wherein step (d) comprises transmitting a received command on the first multimaster bus when the bridge ID in the received command is outside the range of bridge IDs.

36. The method of claim 34 wherein a register in the first unidirectional bridge device holds a first bridge ID value and a register in the second unidirectional bridge device holds a second bridge value different from the first bridge ID value.

37. The method of claim 36 wherein each command contains a bridge ID value and wherein step (b) comprises responding to a command when the bridge ID value therein equals the bridge ID in the first register.

38. The method of claim 37 wherein each command contains a bridge ID value and wherein step (d) comprises responding to a command when the bridge ID value therein equals the bridge ID in the first register.